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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,081	06/25/2003	John W. Horigan	42P16970	6540

8791 7590 10/14/2005

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EXAMINER	
HOLTON, STEVEN E	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,081	HORIGAN, JOHN W.	
	Examiner	Art Unit	
	Steven E. Holton	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art – or – Related Art -- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,2,5-8,11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (paragraphs 4-6 of the disclosure), hereinafter AAPA, in view of Beale et al. (USPN: 5790615), hereinafter Beale.

Regarding claim 1, AAPA discloses a prior method of generating a pixel stream from a non-SSC clock (paragraph 5, lines 1-2) and forwarding a second clock signal and the first pixel stream to a buffer to translate the first pixel stream based on the

second clock signal (paragraph 5, lines 2-4). The Examiner notes that the AAPA does not expressly state if the clocks come from one or two sources, the use of two sources would be obvious to one skilled in the art. However, AAPA does not expressly disclose providing a feedback to the second source to cause the second source to adjust the center frequency of the second clock signal to match the average frequency of the first clock signal with the average frequency of the second clock signal.

Beale discloses a feedback system with two clock signals from different sources (Fig. 3, elements 102 and 104, CLK1 and CLK2) and a data buffer (Fig. 3, element 32). The feedback system works such that based on a count of the amount of data within the buffer (Fig. 3, element 120) the second clock signal is altered to match the average frequency of the first clock signal (col. 8, lines 28-35 (mention of matching average rate (frequency)); col. 9 line 58- col. 10, line 64 (detailed discussion of feedback system)).

At the time of invention it would have been obvious for one skilled in the art to combine a standard twin mode pixel stream system of AAPA with a known problem of buffer overflow/underflow caused by clock signal differences with a feedback system to match the average frequency of the two clock signals such as used by Beale. The motivation for doing so would have been to correct the problem as noted with the AAPA (paragraph 5, lines 8-12) with a system intended to "maintain sample-clock timing synchronization to thereby correct the integration effects on the timing synchronization pulse (Beale, col. 2, lines 58-61)". Thus, it would have been obvious to combine AAPA and Beale to produce a method of operating a device as specified in claim 1.

Regarding claim 2, Beale discloses "sending a signal from the buffer to the second source when the content of the buffer reaches a predetermined threshold value (col. 10, lines 28-42)."

Regarding claim 5, AAPA discloses using a non-spread spectrum modulation clock signal (paragraph 5, lines 1-2) and a spread spectrum modulation clock signal (paragraph 5, lines 2-3).

Regarding claim 6, AAPA discloses sending the pixel stream associated with the non-spread spectrum [first pixel stream] to a cathode ray tube display (paragraph 4, lines 6-8) and a pixel stream associated with the spread spectrum clock signal to a liquid crystal display panel (paragraph 4, lines 3-4).

Regarding claim 7, the Examiner notes that this is an apparatus to be operated using the associated method of claim 1. Although there is no provided figure of a display system that would operate as described by AAPA, the Examiner states that the system would inherently possess a first and second circuitry to produce first and second clock signals; a display pipe to generate a first pixel stream based on the first clock signal; and a buffer coupled to the display pipe to receive the first pixel stream and the second clock signal to transform the first pixel stream into a second pixel stream on the second clock signal. The Examiner notes that no specific mention of a display pipe is made in the AAPA, but there would inherently be some device to produce the pixel stream and such a device could be a display pipe, which is known in the art. AAPA does not expressly disclose the second circuitry being coupled to the buffer to receive a feedback, to adjust the center frequency of the second clock signal.

Beale discloses a first circuitry to generate a first clock signal (fig. 3, element 102; col. 8, lines 60-63), a buffer to receive an input data stream and a second clock signal to transform the data stream into a second output data stream on the second clock signal (fig. 3, element 32; col. 9 line 58 - col. 10, line 64). Beale also discloses circuitry for generating the data used to input into the buffer (Fig. 1, elements 14,16,18, 20, and 30), and using the feedback system to change match the average frequency of the first and second clock signals (col. 8, lines 28-35 (mention of matching average rate (frequency)); col. 9 line 58- col. 10, line 64 (detailed discussion of feedback system)).

At the time of invention it would have been obvious for one skilled in the art to combine a standard twin mode pixel stream system of AAPA with a known problem of buffer overflow/underflow caused by clock signal differences with a feedback system to match the average frequency of the two clock signals such as used by Beale. The motivation for doing so would have been to correct the problem as noted with the AAPA (paragraph 5, lines 8-12) with a system intended to "maintain sample-clock timing synchronization to thereby correct the integration effects on the timing synchronization pulse (Beale, col. 2, lines 58-61)". Thus, it would have been obvious to combine AAPA and Beale to produce a device as specified in claim 7.

Regarding claim 8, Beale discloses "sending a signal from the buffer to the second source when the content of the buffer reaches a predetermined threshold value (col. 10, lines 28-42)."

Regarding claim 11, AAPA discloses using a non-spread spectrum modulation clock signal (paragraph 5, lines 1-2) and a spread spectrum modulation clock signal (paragraph 5, lines 2-3).

Regarding claim 12, AAPA discloses sending the pixel stream associated with the non-spread spectrum [first pixel stream] to a cathode ray tube display (paragraph 4, lines 6-8) and a pixel stream associated with the spread spectrum clock signal to a liquid crystal display panel (paragraph 4, lines 3-4).

Regarding claim 13, the Examiner notes that the claim is drawn to a system comprising the device of claim 7 coupled to dynamic random access memory. Therefore, the arguments of claim 7 can be applied to the similar components of claim 13. Regarding the dynamic random access memory, the Examiner states that in a computer system which is what the graphics apparatus of claim 7 would be used in dynamic random access memory (DRAM) would be an inherent and obvious part of the computer system. DRAM is conventionally used to store program and graphics information in an operating computer system and having it coupled to the graphics controller of claim 7 would be an obvious choice for one skilled in the art.

Thus, the addition of DRAM to the device of claim 7 would have been obvious to one skilled in the art to provide storage for graphics information that would be used by the apparatus of claim 7 to produce pixel streams and other operating information for the computer system.

Regarding claim 14, Beale discloses "sending a signal from the buffer to the second source when the content of the buffer reaches a predetermined threshold value (col. 10, lines 28-42)."

Regarding claim 17, AAPA discloses using a non-spread spectrum modulation clock signal (paragraph 5, lines 1-2) and a spread spectrum modulation clock signal (paragraph 5, lines 2-3).

Regarding claim 18, AAPA discloses sending the pixel stream associated with the spread spectrum clock signal [second pixel stream] to a liquid crystal display panel (paragraph 4, lines 3-4).

Regarding claim 19, AAPA discloses sending the pixel stream associated with the non-spread spectrum [first pixel stream] to a cathode ray tube display (paragraph 4, lines 6-8).

Regarding claim 20, the Examiner notes that the graphics memory controller hub is used within a computer system. As such, it would be obvious to one skilled in the art that the hub would be coupled to a processor that is part of the external computer system. The external processor would be in charge of the computer functions and programs running on the computer.

3. Claims 1, 3, 4, 7,9,10, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Nelson (USPN: 4639680).

Regarding claim 1, as discussed in the above rejection, AAPA discloses the limitations of claim 1 except "providing a feedback to the second source to cause the

second source to adjust the center frequency of the second clock signal to match the average frequency of the first clock signal with the average frequency of the second clock signal".

Nelson discloses a feedback system to correct differences in frequency and phase between two clock sources (col. 2, lines 3-51). The two clock sources being a detector input signal (Fig. 2, element 12) and a square wave (Fig. 2, element 13). Wherein the second clock signal (square wave) is changed based on the signals from the feedback system of Nelson (col. 4, lines 42-59).

At the time of invention it would have been obvious to one skilled in the art to combine the teachings of AAPA and Nelson to produce a device as specified in claim 1. The motivation for doing so would have been to correct the problems caused by the clock frequencies being different as noted by the AAPA. Nelson is described as one method of correcting differences between clock signals requiring no multiplication or signal squaring to filter and process error correcting signals (col. 1, lines 38-45 and 64-68).

Regarding claim 3, Nelson discloses a system with counters (Fig. 2, elements 17, 18), which are used to count the clock pulses (col. 2, lines 12-15; col. 3, line 48 – col. 4, line 12). And the output of the counting system is used to determine the differences between the clock pulses of the two sources to alter the operation of the second clock signal (col. 4, lines 42-59). The Examiner also notes that not every clock pulse is counted, but counts of the first clock pulses are made when the second clock is enabled. Thus, each second clock pulse is counted by the number of times the

counters are enabled, and the first clock pulse is counted directly by the counters. Differences between the two clock signals are derived by the differences of the number of clock pulses during a counting cycle.

Regarding claim 4, Nelson discloses using a phase lock loop as part of the generation of the reference clock signal (col. 4, lines 1-5).

Regarding claim 7, which is an apparatus to function using the associated method of claim 1. Although there is no provided figure of a display system that would operate as described by AAPA, the Examiner states that the system would inherently possess a first and second circuitry to produce first and second clock signals; a display pipe to generate a first pixel stream based on the first clock signal; and a buffer coupled to the display pipe to receive the first pixel stream and the second clock signal to transform the first pixel stream into a second pixel stream on the second clock signal. The Examiner notes that no specific mention of a display pipe is made in the AAPA, but there would inherently be some device to produce the pixel stream and such a device could be a display pipe, which is known in the art. AAPA does not expressly disclose the second circuitry being coupled to the buffer to receive a feedback, to adjust the center frequency of the second clock signal.

Nelson discloses circuitry to provide a feedback system to correct differences in frequency and phase between two clock sources (col. 2, lines 3-51). The two clock sources being a detector input signal (Fig. 2, element 12) and a square wave (Fig. 2, element 13). Wherein the second clock signal (square wave) is changed based on the signals from the feedback system of Nelson (col. 4, lines 42-59).

At the time of invention it would have been obvious to one skilled in the art to combine the teachings of AAPA and Nelson to produce a device as specified in claim 1. The motivation for doing so would have been to correct the problems caused by the clock frequencies being different as noted by the AAPA. Nelson is described as one method of correcting differences between clock signals requiring no multiplication or signal squaring to filter and process error correcting signals (col. 1, lines 38-45 and 64-68).

Regarding claim 9, Nelson discloses a system with counters (Fig. 2, elements 17, 18), which are used to count the clock pulses (col. 2, lines 12-15; col. 3, line 48 – col. 4, line 12). And the output of the counting system is used to determine the differences between the clock pulses of the two sources to alter the operation of the second clock signal (col. 4, lines 42-59). The Examiner also notes that not every clock pulse is counted, but counts of the first clock pulses are made when the second clock is enabled. Thus, each second clock pulse is counted by the number of times the counters are enabled, and the first clock pulse is counted directly by the counters. Differences between the two clock signals are derived by the differences of the number of clock pulses during a counting cycle.

Regarding claim 10, Nelson discloses using a phase lock loop as part of the generation of the reference clock signal (col. 4, lines 1-5).

Regarding claim 13, the Examiner notes that the claim is drawn to a system comprising the device of claim 7 coupled to dynamic random access memory. Therefore, the arguments of claim 7 can be applied to the similar components of claim

13. Regarding the dynamic random access memory, the Examiner states that in a computer system which is what the graphics apparatus of claim 7 would be used in dynamic random access memory (DRAM) would be an inherent and obvious part of the computer system. DRAM is conventionally used to store program and graphics information in an operating computer system and having it coupled to the graphics controller of claim 7 would be an obvious choice for one skilled in the art.

Thus, the addition of DRAM to the device of claim 7 would have been obvious to one skilled in the art to provide storage for graphics information that would be used by the apparatus of claim 7 to produce pixel streams and other operating information for the computer system.

Regarding claim 15, Nelson discloses a system with counters (Fig. 2, elements 17, 18), which are used to count the clock pulses (col. 2, lines 12-15; col. 3, line 48 – col. 4, line 12). And the output of the counting system is used to determine the differences between the clock pulses of the two sources to alter the operation of the second clock signal (col. 4, lines 42-59). The Examiner also notes that not every clock pulse is counted, but counts of the first clock pulses are made when the second clock is enabled. Thus, each second clock pulse is counted by the number of times the counters are enabled, and the first clock pulse is counted directly by the counters. Differences between the two clock signals are derived by the differences of the number of clock pulses during a counting cycle.

Regarding claim 16, Nelson discloses using a phase lock loop as part of the generation of the reference clock signal (col. 4, lines 1-5).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Giemborek et al. (USPgPub: 2003/0222876) claims a broad method of altering a clock signal to match another clock signal for graphics processing. Vermeulen et al. (USPN: 5453790) discloses a method of keeping an input buffer from under and overflow. Horvath et al. (USPN: 6754745) and Kou et al. (USPN: 6154225) disclose methods of reducing clock signals to keep buffer output from overflowing. Mack et al. (USPN: 4001690) discloses altering an input clock to a buffer to avoid overflow rather than an output clock signal. Chee (USPN: 5694141) discloses using direct requests for more data based on the level of data within a buffer to avoid underflow and overflow rather than manipulating clock signals.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven E. Holton whose telephone number is (571) 272-7903. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven E. Holton
October 7, 2005
Art Unit 2673

VIJAY SHANKAR
PRIMARY EXAMINER